



PTO/SB/08a/b (08-03)

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Complete If Known**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet	1	of	1	Attorney Docket Number	SCEI 3.0-200
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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (# known)			
SS	AA	US-5,274,797	12/28/1993	Barlow et al.	
SS	AB	US-5,715,184	02/03/1998	Tyler et al.	
SS	AC	US-5,761,516	06/02/1998	Rostoker et al.	
SS	AD	US-2002/0053684 A1	05/09/2002	Chauvel et al.	
SS	AE	US-2002/0065049 A1	05/30/2002	Chauvel et al.	
SS	AF	US-2003/0125900 A1	07/03/2003	Orenstien et al.	

FOREIGN PATENT DOCUMENTS

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		Country Code ³ -Number ⁴ -Kind Code ⁵ (# known)				

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
SS	CA	Azevedo et al., "Architectural and Complier Strategies for Dynamic Power Management in the COPPER Project," 2001 International Workshop on Innovative Architecture, January 2001.	
SS	CB	Heo et al., "Reducing Power Density through Activity Migration," Proceedings of the 2003 International Symposium on Low Power Electronics and Design (ACM Press, ©2003), pp. 217-222.	
SS	CC	Tiwari et al., "Instruction Level Power Analysis and Optimization of Software," Journal of VLSI Signal Processing, Vol. 13, No. 2 (August 1996), pp. 1-18.	
SS	CD	Abhishek Mehta, "Techniques for Low Power Processing - A Survey" CSE 822, Spring 2001, A29838087, Retrieved from the Internet on March 29, 2004, <URL: www.cs.vcr.edu/~chzhang/papers_read/lowpower_survey.pdf >; 10 pages.	
SS	CE	Lee et al., "Power Analysis and Minimization Techniques for Embedded DSP Software," IEEE Transactions on VLSI Systems, Vol. 5, No. 1, March 1997, pp. 123-135 (manuscript copy submitted).	
SS	CF	Gerosa et al., "A 250-MHz 5-W PowerPC Microprocessor with On-Chip L2 Cache Controller," IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997, pp. 1635-1649.	

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Examiner Signature	/Stefan Stoynov/	Date Considered	12/23/2006
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Sheet	1	of	1	Attorney Docket Number	SCEI 3.0-200
Application Number	10/812,155-Conf. #2941				
Filing Date	March 29, 2004				
First Named Inventor	Keisuke Inoue				
Art Unit	2115				
Examiner Name	Not Yet Assigned				

U.S. PATENT DOCUMENTS

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SS	AA*	US-2003/0079151-A1	04-24-2003	Bohrer et al.	
SS	AB*	US-2003/0115495-A1	06-19-2003	Rawson, III	
SS	AC*	US-5,745,778	04-28-1998	Alfieri	

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SS	BA	WO-03/025745-A2	03-27-2003	International Business Machines Corporation		
SS	BB	EP-1 182 552-A2	02-27-2002	Texas Instruments France; Texas Instruments Incorporated		

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SS	CA	PINHEIRO, EDUARDO, ET AL., "Load Balancing and Unbalancing for Power and Performance in Cluster-Based Systems," 10th International Conference on Parallel Architectures and Compilation Techniques, May 2001	
SS	CB	ELNOZAHY, E.N., ET AL., "Energy-Efficient Server Clusters," Proceedings of the Workshop on Power-Aware Computing Systems, Feb. 2, 2002.	

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Examiner Signature 642706	/Stefan Stoynov/	Date Considered	12/23/2006
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Complete if Known

Application Number	10/812,155-Conf. #2941
Filing Date	March 29, 2004
First Named Inventor	Keisuke Inoue
Art Unit	2115
Examiner Name	T. C. Lee

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		Number-Kind Code ² (if known)			
SS	AA*	US-2003/0110012-A1	10-12-2004	Orenstien et al.	
SS	AB*	US-2003/0229662-A1	12-11-2003	Luick	
SS	AC*	US-2005/0278520-A1	12-15-2005	Hirai et al.	
SS	AD*	US-2004/0003309-A1	01-01-2004	Cai et al.	
SS	AE*	US-6,269,043-B1	07-31-2001	Batcher	
SS	AF*	US-6,192,479-B1	02-20-2001	Ko	

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		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
SS	BA	WO-03/083693-A	10-09-2003	FUJITSU LIMITED		**
SS	BB	JP-08-016531-A	01-19-1996	HITACHI LTD		**
SS	BC	JP-10-240704-A	09-11-1998	RICOH CO LTD		**

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SS	CA	SEONGMOO HEO et al, "Reducing Power Density Through Activity Migration", Proceedings of the 2003 International Symposium on Low Power Electronics and Design, Seoul, Korea, Aug. 25-27, 2003.	**

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** - English abstract attached.

Examiner Signature 658892	/Stefan Stoynov/	Date Considered	12/23/2006
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